Claims

[c1] What is claimed is:

1.A method of forming a metal-oxide semiconductor (MOS) transistor with a shallow junction in nitride read only memory (NROM), the method comprising:

providing a semiconductor wafer with both a memory array area and a periphery circuit region defined on a surface of a substrate of the semiconductor wafer;

forming a silicon oxide layer on the surface of the periphery circuit region;

forming a silicon germanium layer on the surface of the silicon oxide layer;

patterning the silicon germanium layer to form a gate of the MOS transistor on the surface of the substrate;

forming a spacer around the gate;

forming a source and a drain of the MOS transistor in the substrate;

forming a nickel (Ni) layer on the surface of the source and the drain; and

performing a rapid thermal annealing process (RTA process) to react the nickel layer with the surface of the source and the drain to form a silicon nickel layer.

[c2] 2.The method of claim 1 wherein the silicon germanium layer comprising a chemical composition of $Si_{1-x}Ge_{x}$, with x = 0.05 to 1.0.

[c3] 3.The method of claim 1 wherein patterning the silicon germanium layer further patterning the silicon oxide layer.

[c4] 4.The method of claim 1 wherein the silicon oxide layer functions as a gate oxide layer of the MOS transistor.

[c5] 5.The method of claim 1 wherein the MOS transistor is an NMOS transistor or a PMOS transistor.

[c6] 6.The method of claim 1 further comprising a first ion implantation process for forming a lightly doped drain (LDD) of the MOS transistor.

[c7] 7.The method of claim 1 wherein forming the source and the drain comprises:

performing a second ion implantation process to form two doping areas on the substrate adjacent to two related sides of the gate; and

performing a thermal annealing process to drive dopants into the two doping areas to form the source and drain.

[c8] 8.The method of claim 1 wherein the substrate is a silicon substrate.

[c9] 9.The method of claim 8 wherein the silicon nickel layer formed by reacting the nickel layer with the surface of the source and the drain consumes silicon atoms in the silicon substrate so as to form a shallow junction of the source and the drain.

[c10] 10. The method of claim 1 wherein the silicon germanium layer is formed by performing a chemical vapor deposition (CVD) process utilizing silane (SiH_4), germane (GeH_4) and hydrogen at a temperature ranging between 450 ° C and 620 ° C.

[c11] 11.The method of claim 1 wherein a plurality of NROM memory cells are formed in the memory array area, and each NROM memory cell comprises a MOS transistor and a silicon nitride layer.

[c12] 12.A method of forming a metal-oxide semiconductor (MOS) transistor with a shallow junction, the method comprising:
providing a semiconductor wafer;
forming a silicon oxide layer on a silicon substrate of the semiconductor wafer;
performing an in-situ doped chemical vapor deposition (CVD) process for forming a silicon germanium layer on the surface of the silicon oxide layer;
patterning the silicon germanium layer to form a gate of the MOS transistor on the surface of the silicon substrate;
forming a spacer around the gate;
performing a first ion implantation process to form two doping areas on the silicon substrate adjacent to two related sides of the gate;
performing a thermal annealing process to drive dopants into the two doping areas to form a source and a drain of the MOS transistor;
forming a nickel (Ni) layer on the surface of the source and the drain; and
performing a rapid thermal annealing process (RTA process) to react the nickel layer with the surface of the source and the drain to form a silicon nickel layer on the surface of the source and the drain.

[c13] 13.The method of claim 12 wherein patterning the silicon germanium layer

further patterning the silicon oxide layer.

[c14] 14.The method of claim 12 wherein the silicon oxide layer functions as a gate oxide layer of the MOS transistor.

[c15] 15.The method of claim 12 wherein the MOS transistor is an NMOS transistor or a PMOS transistor.

[c16] 16.The method of claim 12 further comprising a second ion implantation process for forming a lightly doped drain (LDD) of the MOS transistor.

[c17] 17.The method of claim 12 wherein process gases of the in-situ doped CVD process comprise silane (SiH_4), germane (GeH_4) and hydrogen, and the process temperature of the in-situ doped CVD process ranges between 450 °C and 620 °C.